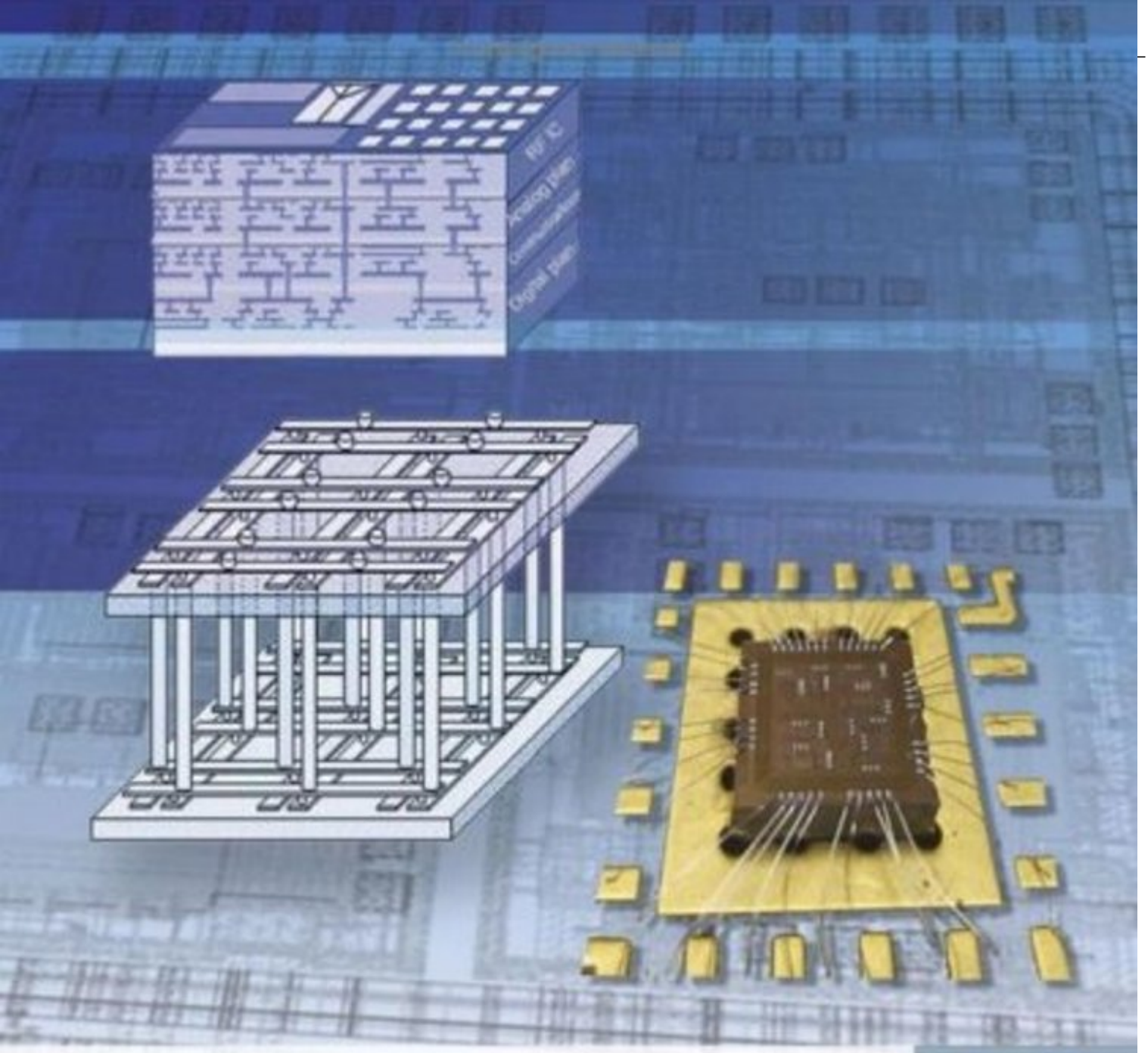

THREE-DIMENSIONAL INTEGRATED CIRCUIT DESIGN

SYSTEMS ON SILICON

VASILIS F. PAVLIDIS EBY G. FRIEDMAN

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MORGAN KAUFMANN

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To the memory of my beloved grandfathers, Athanasios Theophilidis and Vasileios Pavlidis

To my wife and lifelong companion, Laurie. LL

Preface

The seminal reason for this book is the lack of a unified treatment of the design of three-dimensional integrated circuits despite the significant progress that has recently been achieved in this exciting new technology. Consequently, the intention of this material is to cohesively integrate and present research milestones from different, yet interdependent, aspects of three-dimensional integrated circuit design. The foremost goal of the book is to propose design methodologies for 3-D circuits; methodologies that will effectively exploit the flourishing manufacturing diversity existing in three-dimensional integration. While the focal point is design techniques and methodologies, the material also highlights significant manufacturing strides that complete the research mosaic of three-dimensional integration.

Three-dimensional or vertical integration is an exciting path to boost the performance and extend the capabilities of modern integrated circuits. These capabilities are inherent to three-dimensional integrated circuits. The former enhancement is due to the considerably shorter interconnect length in the vertical direction and the latter is due to the ability to combine dissimilar technologies within a multi-plane system. It is also worth noting that vertical integration is particularly compatible with the integrated circuit design process that has been developed over the past several decades. These distinctive characteristics make three-dimensional integration highly attractive as compared to other radical technological solutions that have been proposed to resolve the increasingly difficult issue of on-chip interconnect.

The opportunities offered by three-dimensional integration are essentially limitless. The constraints stem from the lack of design and manufacturing expertise for these circuits. The realization of these complex systems requires advanced manufacturing methods and novel design technologies across several abstraction levels. The development of these capabilities will be achieved if the physical behavior and mechanisms that govern interplane communication and manufacturing are properly understood. The focus of this book diligently serves this purpose.

This book is based upon the body of research carried out by Vasilis Pavlidis from 2002 to 2008 at the University of Rochester during his doctoral study under the supervision of Professor Eby G. Friedman. Recognizing the importance of the vertical interconnections in 3-D circuits, these structures are central to the content of this book. Tutorial chapters are dedicated to manufacturing processes, technological challenges, and electrical models of these structures. The vertical wires are investigated not only as a communication medium but also as heat conduits within the 3-D system. From this perspective, novel and efficient algorithms are presented for improving the signal propagation delay of heterogeneous three-dimensional systems that consider the electrical

behavior of the vertical interconnects. Additionally, the important role that the vertical interconnects play in global signaling and thermal amelioration is described. Measurements from a case study of a 3-D circuit increase the physical understanding and intuition of this critical interconnect structure.

The short vertical wires enable several 3-D architectures for communication centric circuits. Opportunities for improved communication bandwidth, enhanced latency, and low power in 3-D systems are investigated. Analytic models and exploratory tools for these architectures are also discussed. The intention of this part of the book is to illuminate important design issues while providing guidelines for designing these evolving 3-D architectures.

The organization of the book is based on a bottom-up approach with technology and manufacturing of 3-D systems as the starting point. The first two chapters cover the wide spectrum of available 3-D technologies and related fabrication processes. These chapters demonstrate the multi-technology palette that is available in designing a 3-D circuit. Based on these technologies and *a priori* interconnect models, projections of the capabilities of 3-D circuits are provided. Physical design methodologies for 3-D circuits, which are the core of this book, are considered in the next eight chapters. The added design complexity due to the multi-plane nature of a 3-D system, such as placement and routing, is reviewed. Efficient approaches to manage this complexity are presented. Extensions to multi-objective methodologies are discussed with the thermal issue as a primary reference point. As the vertical interconnects can behave either obstructively or constructively within a 3-D circuit, different design methodologies to utilize these interconnects are extensively discussed. Specific emphasis is placed on the through silicon vias, the important vertical interconnection structure for 3-D circuits. Various 3-D circuit architectures, such as a processor and memory system, FPGAs, and on-chip networks, are discussed. Different 3-D topologies for on-chip networks and FPGAs are explored. Novel algorithms and accurate delay and power models are reviewed. The important topic of synchronization is also investigated, targeting the challenges of distributing a clock signal throughout a multi-plane circuit. Experimental results from a 3-D fabricated circuit provide intuition into this global signaling issue.

Three-dimensional integration is a seminal technology that will prolong the semiconductor roadmap for several generations. The third dimension offers nonpareil opportunities for enhanced performance and functionality; vital requirements for contemporary and future integrated systems. Considerable progress in manufacturing 3-D circuits has been achieved within the last decade. 3-D circuit design methodologies, however, considerably lag these technological advancements. This book ambitiously targets to fill this gap and strengthen the design capabilities for 3-D circuits without overlooking aspects of the fabrication process of this emerging semiconductor paradigm.

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Chapter 1

Introduction

Electronics has experienced tremendous growth over the past century. During this time period, the use of electronic merchandise has steadily increased while the size of these products has decreased. The transition from micro- to nano-scale has further enhanced the applicability of electronic products into new areas, which were previously precluded due to the prohibitive size of these systems. The seed that caused this growth — the "big-bang" of electronics — was a grain of germanium on which the point contact transistor was fabricated for the first time in 1947 by J. Bardeen, W. Brattain, and W. Shockley [1].

This invention appealed to the interests of scientists and engineers, resulting in research efforts focused on developing semiconductor devices to replace the bulky, power-hungry, and low-performance vacuum tubes and electromechanical relays on which much of the electronics of the pre-transistor era were based [2]. This quest led to the emergence of a new branch of electronics, namely, the semiconductor industry, which experienced tremendous growth over the following decades. An important engine behind this explosive evolution was the plethora of semiconductor-based applications. Semiconductor products have ultimately affected every component of our society.

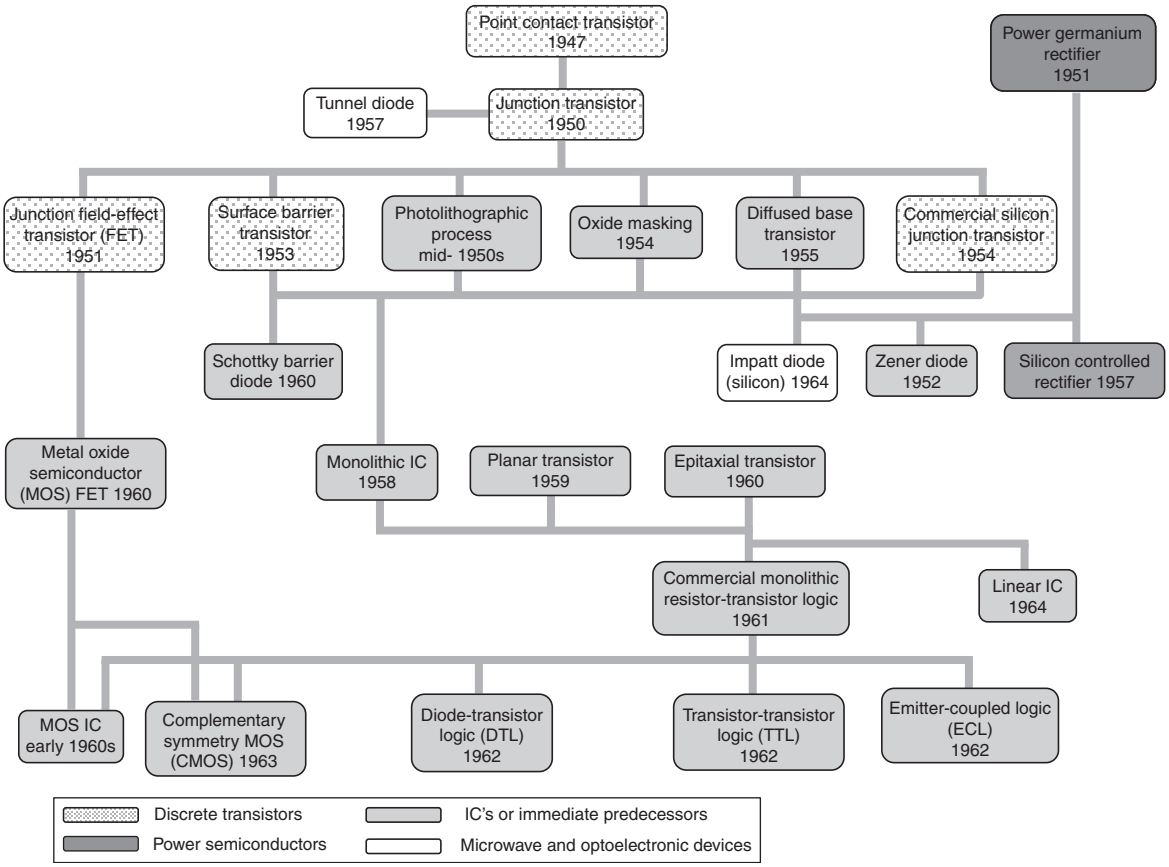
For example, manufacturing was considerably advanced due to automation, reducing the cost and time to market and offering more reliable products, while increasing employee safety through highly sophisticated electronic security systems that can recognize and warn of critical equipment failures [3]. Office automation also significantly simplified the painstaking process of writing letters, memos, and reports, while facilitating filing by offering a variety of storage media [4]. In addition, medical procedures were simplified, and invasive diagnostic methods, which were often dangerous to patients, were replaced by safe and effective noninvasive techniques. Furthermore, minute electronics devices, such

as the pacemaker and hearing aid, enhanced the treatment of myriad patients [5]. Communications is another component of our society that has passed through a revolution during the past several decades. Satellite communications, geographical positioning systems, cell phones, and the Internet are some of the salient achievements in the communications field. Without the robust and powerful transistor, most of these capabilities would be rather primitive, if not impossible.

Science and engineering perhaps benefited the most from the microelectronics revolution and the flourishing semiconductor industry [6]. Computational tasks, once formidable, are now solved in fractions of a second. Numerous computer programs, measurement instrumentation, and observation apparatus have been developed, expanding our knowledge of the environment, nature, and the universe. Information processing and propagation capabilities have been improved by orders of magnitude as compared to the beginning of the twentieth century, making knowledge available in almost any place around the globe. The electronics industry has been, in turn, assisted by these developments, both intellectually and financially. Novel applications further boosted the semiconductor revolution, producing colossal revenues that helped establish and fuel industrial R&D. Some of the milestones of this stupendous progress are described in the following section. Interconnect-related problems since the earliest days of the integrated circuit industry and the impending performance bottleneck caused by the interconnect are discussed in Section 1.2. A promising solution and an important next step in the evolution of the microelectronics field, namely, three-dimensional integration, is introduced in Section 1.3. An outline of this book is presented in Section 1.4.

1.1 FROM THE INTEGRATED CIRCUIT TO THE COMPUTER

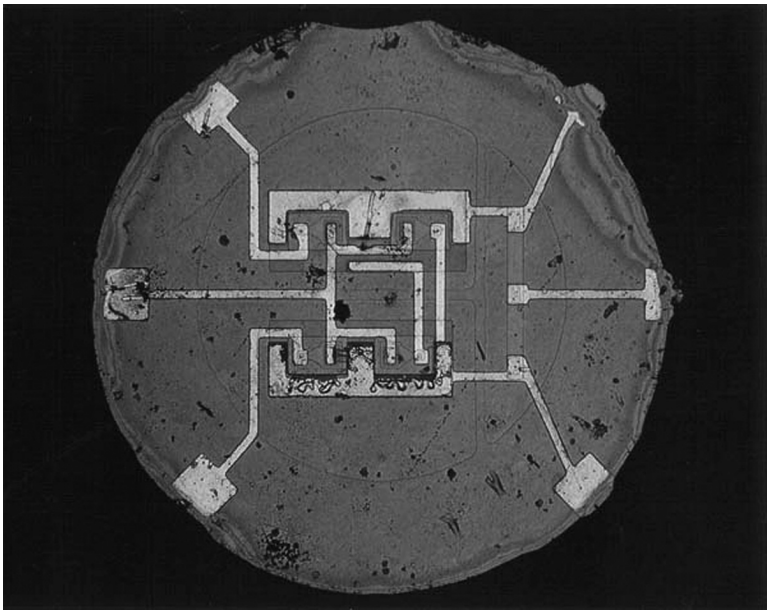
During the years that followed the genesis of the point contact transistor in 1947, several different types of semiconductor devices were fabricated to satisfy a variety of important applications in control systems, military, medicine, and a host of other areas. A time line of these inventions is shown in Figure 1-1. These transistors were discrete components connected together with traces of metal that implemented different circuit functions. Although these innovative devices could perform better and more reliably at greater frequencies than vacuum tubes or other electromechanical equipment, a system that exclusively consisted of discrete components would be of limited performance and could not exploit the



■ **FIGURE 1-1** History of transistor generations and logic styles [8].

full potential of semiconductor devices. Not until the development of the planar process in 1960, which resulted in the familiar integrated circuit, as shown in Figure 1-2, could the capabilities of the transistor begin to be fully utilized [7]. This achievement reinforced the growth of the semiconductor industry, offering a large number of devices integrated within the silicon, implementing a vast variety of circuit functions.

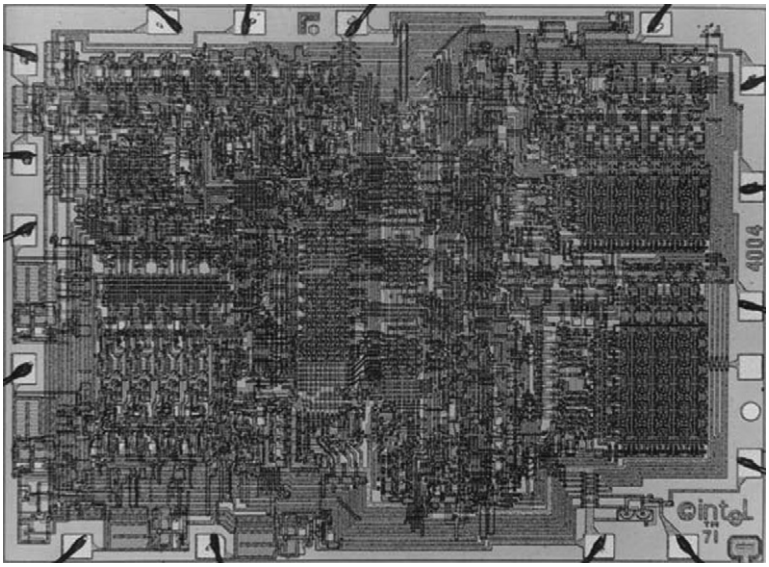
Later improvements in the fabrication process and integration on inexpensive silicon resulted in integrated circuits (ICs) with higher yield and hence lower cost, greater performance, and enhanced reliability. Within the next decade, several logic-style families such as transistor-transistor logic (TTL), emitter-coupled logic (ECL), and complementary metal oxide semiconductor (CMOS) were proposed. As the complexity



■ **FIGURE 1-2** The first planar integrated circuit [9].

of the ICs increased, a profound need developed for circuits suitable for generalized applications. Indeed, thus far, each IC was designed to serve a single application, requiring companies to design a variety of low-cost components to maintain profitability. The answer to this profound need was provided by M. E. Hoff Jr., an engineer at Intel. He envisioned a more flexible way to utilize the capabilities of these integrated circuits. Encouraged by the founders of Intel, Gordon Moore and Robert Noyce, the result of this effort was the first microprocessor, namely, the 4004, which is illustrated in Figure 1-3. This 0.11×0.15 square inch IC could execute addition and multiplication with four-bit numbers, while a bank of registers was used for storage purposes. Although this capability seems trivial today, the 4004 microprocessor fundamentally altered the way that computers were perceived and used.

Since the 4004 was announced in 1971, microprocessors and ICs in general have steadily improved, demonstrating higher performance and reliability. This fascinating trajectory was essentially driven by the maturation of the semiconductor manufacturing process, supported by the continued scaling of the transistors. The merits of this evolution were foreseen quite early by Moore and Noyce, as discussed in the following section, where the physical limitations of technology scaling are also described.



■ **FIGURE 1-3** The 4004 Intel microprocessor [9].

1.2 **INTERCONNECTS, AN OLD FRIEND**

During the infancy of the semiconductor industry, the connections among the active devices of a circuit presented an important obstacle for increasing circuit performance. The significant capacitance of the interconnects necessitated large power drivers and hindered a rapid increase in performance that could be achieved by the transistors. Noyce had already noticed the importance of the interconnects, such as the increase in delay and noise due to coupling with neighboring interconnects [10]. The invention of the integrated circuit considerably alleviated these early interconnect-related problems by bringing the interconnects on-chip. The interconnect length was significantly reduced, decreasing the delay and power consumption while reducing the overall cost. From a performance point of view, the speed of the transistors dominated the overall delay characteristics. Over the next three decades, on-chip interconnects were not the major focus of the IC design process, as performance improvements reaped from scaling the devices were much greater than any degradation caused by the interconnects.

With continuous technology scaling, however, the interconnect delay, noise, and power grew in importance [11], [12]. A variety of methodologies at the architectural, circuit, and material levels has been

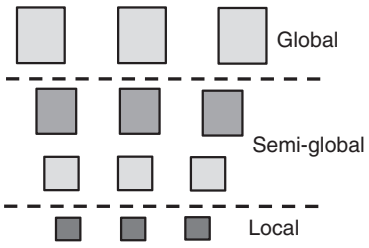
developed to address these interconnect design objectives. At the material level, manufacturing innovations such as the introduction of copper interconnects and low-k dielectric materials helped to prolong the improvements in performance gained from scaling [13]–[17]. This situation is due to the lower resistivity of the copper as compared to aluminum interconnects and the lower dielectric permitivity of the new insulator materials as compared to silicon dioxide.

Multitier interconnect architectures [18], [19], shielding [20], wire sizing [21], [22], and repeater insertion [23] are only a handful of the many methods employed to cope with interconnect issues at the circuit level. Multitier interconnect architectures, for example, support tiers of metal layers with different cross sections [19], as illustrated in Figure 1-4. Each tier typically consists of multiple metal layers routed in orthogonal directions with the same cross section. The key idea of this structure is to utilize wires of decreasing resistance to connect those circuits located farther away. Thus, the farther the distance among the circuits, the thicker the wires used to connect these circuits. The increase in the cross section of the wires is shown in Figure 1-4. The thickness of the tiers, however, is limited by the fabrication technology and related reliability and yield concerns.

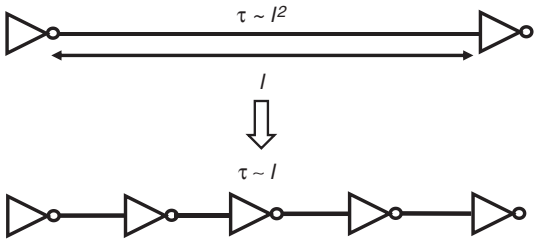
Varying the width of the wires, also known as wiring sizing, is another means to manage the interconnect characteristics. Wider wires lower the interconnect resistance, decreasing the attenuative properties of the wire. Although wire sizing typically has an adverse effect on the power consumed by the interconnect, proper sizing techniques can also decrease the power consumption [22], [24].

Other practices do not modify the physical characteristics of the propagation medium. Rather, by introducing additional circuitry and wire resources, the performance and noise tolerance of an interconnect system can be enhanced. For instance, in a manner similar to the use of repeaters in telephone lines systems, a properly designed interconnect system with buffers (also known as repeaters) amplifies the attenuated signals, recovering the originally transmitted signal that is propagated along a line. Repeater insertion effectively converts the square dependence of the delay on the interconnect length to a linear function of length, as shown in Figure 1-5.

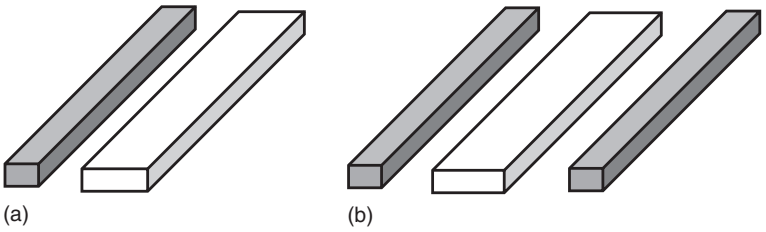
Shielding is an effective technique to reduce crosstalk among adjacent interconnects. Single- or double-sided shielding, as depicted in Figure 1-6, is commonly utilized to improve signal integrity. Shields can also improve interconnect delay and power, particularly in buss



■ **FIGURE 1-4** Interconnect architecture including local, semi-global, and global tiers. The metal layers on each tier are of different thicknesses.



■ **FIGURE 1-5** Repeaters are inserted at specific distances to improve the interconnect delay.



■ **FIGURE 1-6** Interconnect shielding to improve signal integrity: (a) single-sided and (b) double-sided shielding. The shield and signal lines are illustrated by the grey and white color, respectively.

architectures, in addition to mitigating noise. Careful tuning of the relative delay of the propagated signals [25] and signal encoding schemes [26] are other strategies to maintain signal integrity. Despite the benefits of these techniques, issues arise such as the increase in power consumption, greater routing congestion, the reduction of wiring resources, and an increase in area.

At higher abstraction levels, pipelining the global interconnects and employing error-correction mechanisms can partially improve the performance and fault tolerance of the wires. The related cost of these architecture level techniques in terms of area and design complexity, however, increases considerably. Other interconnect schemes such as current mode signaling [27], wave pipelined interconnects [28], and low swing signaling [29] have been proposed as possible solutions to the impending interconnect bottleneck. These incremental methods, however, have limited ability to reduce the length of the wire, which is the primary cause of the deleterious behavior of the interconnect.

Novel design paradigms are therefore required that do not impede the well-established and historic improvement in performance in next-generation integrated circuits. Canonical interconnect structures that utilize Internet-like packet switching for data transfer [30], optical interconnects [31], and three-dimensional integration are possible

solutions for providing communication among devices or functional blocks within an IC.

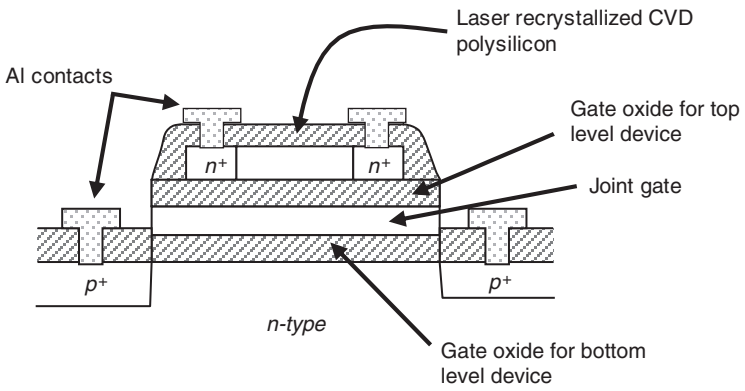
On-chip networks can considerably enhance the communication bandwidth among the individual functional blocks of an integrated system, since each of these blocks utilizes the resources of the network. In addition, noise issues are easier to manage as the layered structure of the communication protocols utilized within on-chip networks provides error correction. The speed and power consumed by these networks, however, are eventually limited by the delay of the wires connecting the network links.

Alternatively, on-chip optical interconnects can greatly improve the speed and power characteristics of interconnects within an integrated circuit, replacing the critical electrical nets with optical links [32], [33]. On-chip optical interconnects, however, remain a technologically challenging problem. Indeed, integrating a modulator and detector onto the silicon within a standard CMOS process is a difficult task [31]. In addition, the detector and modulator should exhibit performance characteristics that ensure the optical links outperform the electrical interconnects [33]. Furthermore, an on-chip optical link consumes a larger area as compared to a single electrical interconnect line. To limit the area consumed by the optical interconnect, multiplexing the optical signals (wavelength division multiplexing (WDM)) can be exploited. On-chip WDM, however, imposes significant challenges.

Volumetric integration by exploiting the third dimension greatly improves the interconnect performance characteristics of modern integrated circuits, while the interconnect bandwidth is not degraded. In general, three-dimensional integration should not be seen as competitive but rather synergistic with on-chip networks and optical interconnections. The unique opportunities that three-dimensional integration offers to the circuit design process and the challenges that arise from the increasing complexity of these systems are discussed in the following section.

1.3 THREE-DIMENSIONAL OR VERTICAL INTEGRATION

Successful fabrication of vertically integrated devices dates back to the early 1980s [34]. The structures include 3-D CMOS inverters where the positive-channel metal oxide semiconductor (PMOS) and negative-channel metal oxide semiconductor (NMOS) transistors

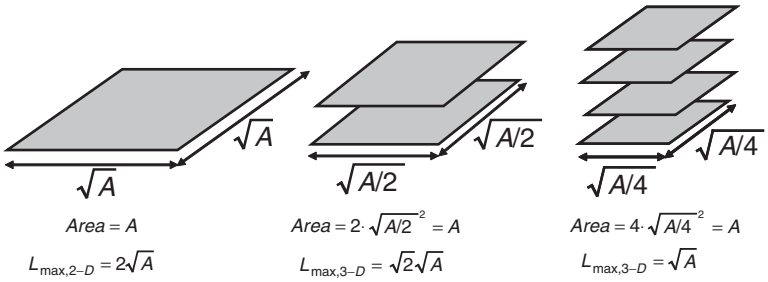


■ **FIGURE 1-7** Cross section of a JMOS inverter [35].

share the same gate, considerably reducing the total area of the inverter, as illustrated in Figure 1-7. The term joint metal oxide semiconductor (JMOS) was used for these structures to describe the joint use of a single gate for both devices [35]. In the following years, research on three-dimensional integration remained an area of limited scientific interest. Due to the increasing importance of the interconnect and the demand for greater functionality on a single substrate, vertical integration has recently become a more prominent research topic. Over the last five years, three-dimensional integration has evolved into a design paradigm manifested at several abstraction levels, such as the package, die, and wafer levels. Alternatively, different manufacturing processes and interconnect schemes have been proposed for each of these abstraction levels [36]. The salient features and important challenges for three-dimensional systems are briefly reviewed in the following subsections.

1.3.1 Opportunities for Three-Dimensional Integration

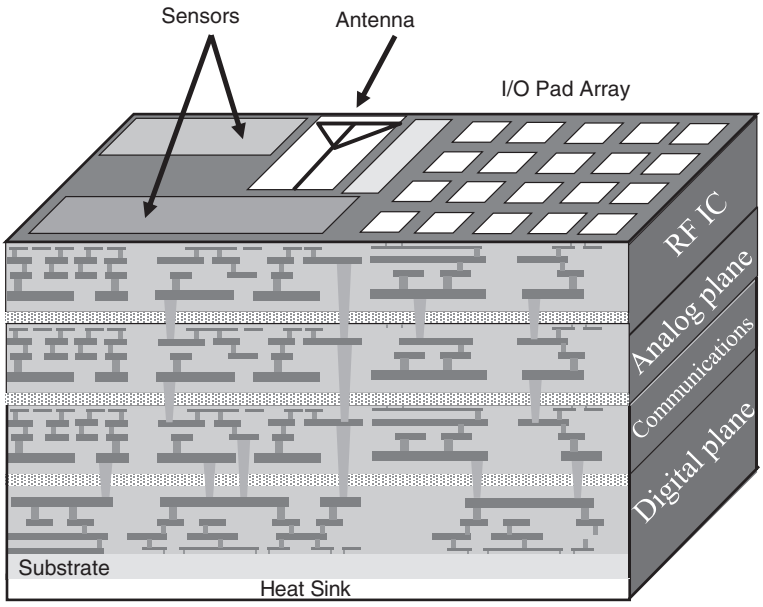
The quintessence of three-dimensional integration is the drastic decrease in the length of the longest interconnects across an integrated circuit. To illustrate this situation, consider the simple example structure shown in Figure 1-8. A common metric to characterize the longest interconnect is to assume that the length of a long interconnect is equal to twice the length of the die edge. Consequently, assuming a planar integrated circuit with an area A, the longest interconnect in a planar IC has a length $L_{\max,2-D} = 2\sqrt{A}$. Implementing the same circuitry onto two bonded dies requires an area $A/2$ for each plane, while the total area of the system remains the same.



■ **FIGURE 1-8** Reduction in wirelength where the original 2-D circuit is implemented in two and four planes.

Hence, the length of the longest interconnect for a two-plane 3-D IC is $L_{\max,3-D} = 2\sqrt{A/2}$. Increasing the number of dies within a 3-D IC to four, the area of each die can be further reduced to $A/4$, and the longest interconnect would have a length of $L_{\max,3-D} = 2\sqrt{A/4}$. Consequently, the wire length exhibits a reduction proportional to $\sqrt{n}$, where n is the number of dies or physical planes that can be integrated into a 3-D system. Although in this simplistic example the effect of the connections among circuits located on different dies is not considered, *a priori* accurate interconnect prediction models adapted for 3-D ICs also demonstrate a similar trend caused by the reduction in wirelength [37]. This considerable decrease in length is a promising solution for increasing the speed while reducing the power dissipated by an IC.

Another characteristic of 3-D ICs of greater importance than the decrease in the interconnect length is the ability of these systems to include disparate technologies. This defining feature of 3-D ICs offers unique opportunities for highly heterogeneous and multifunctional systems. A real-time image processing system in which the image sensor on the topmost plane captures the light, the analog circuitry on the plane below converts the signal to digital data, and the remaining two planes of digital logic process the information from the upper planes is a powerful example of a heterogeneous 3-D system-on-chip (SoC), with considerably improved performance as compared to a planar implementation of the same system [38], [39]. Another example where the topmost plane can include other types of sensors such as seismic and acoustic sensors and an additional plane with wireless communications circuitry is schematically illustrated in Figure 1-9. A vast pool of applications, in the military, medical, and wireless communication domains, as well as low-cost consumer products exists for vertical integration, as the proximity of the system components due to the third dimension is suitable for either the high-performance or low-power ends of the SoC application spectrum.



■ **FIGURE 1-9** An example of a heterogeneous 3-D system-on-chip comprising sensor and processing planes.

1.3.2 Challenges for Three-Dimensional Integration

Developing a design flow for 3-D ICs is a complicated task with many ramifications. A number of challenges at each step of the design process have to be satisfied for 3-D ICs to successfully evolve into a mainstream technology. Design methodologies at the front end and mature manufacturing processes at the back end are required to effectively provide large-scale 3-D systems. Several of the primary challenges to the successful development of 3-D systems are summarized below.

Technological/Manufacturing Limitations

Some of the fabrication issues encountered in the development of 3-D systems concern the reliable lamination of several ICs, possibly from dissimilar technologies. The stacking process should not degrade the performance of the individual planes, while guaranteeing the planes remain bonded throughout the lifetime of the 3-D system. Furthermore, packaging solutions that accommodate these complicated 3-D structures need to be developed. In addition, the expected reduction in wirelength depends on the vertical interconnects utilized to propagate signals and power throughout the planes of a 3-D system.

The technology of the interplane interconnects is a primary determining factor in circuit performance. Consequently, providing high-quality and

highly dense vertical interconnects is of fundamental importance in 3-D circuits; otherwise, the performance or power gains achieved by the third dimension will diminish [40]. Alternatively, the density of this type of interconnect dictates the granularity at which the planes of the system can be interconnected, directly affecting the bandwidth of the interplane communication.

Testing

Manufacturing a 3-D system typically includes bonding multiple physical planes. The stacking process can occur either in a wafer-to-wafer, die-to-wafer, or die-to-die manner. Consequently, novel testing methodologies at the wafer and die level are required. Developing testing methodologies for wafer-level integration is significantly more complicated than die-level testing techniques. The considerable reduction in turnaround time due to the higher integration, however, may justify the additional complexity of these testing methods.

An important distinction between 2- and 3-D IC testing is that in the latter case only part of the functionality of the system is tested at a given time (typically, only one plane is tested at a time). This characteristic requires additional resources, for example, scan registers embedded within each plane. Furthermore, additional interconnect resources, such as power/ground pads, are necessary. These extra pads supply power to the plane during testing. In general, testing strategies for 3-D systems should not only include methodologies for generating appropriate input patterns for each plane of the system, but also minimize the circuitry dedicated to efficiently test each plane within a 3-D stack.

Interconnect Design

Design for test strategies are only a portion of the many design methodologies that need to be developed for 3-D ICs. Interconnect design and analysis of 3-D circuits are also challenging tasks. This capability is primarily due to the inherent heterogeneity of these systems, where different fabrication processes or disparate technologies are combined into a 3-D circuit. Consequently, models that consider the particular traits of 3-D ICs are necessary. In these diverse systems, global interconnect, such as clock and power distribution, grow in importance. Furthermore, well-developed noise mitigation techniques may not be suitable for 3-D circuits. Noise caused by capacitive and inductive coupling of the interconnections between adjacent planes needs to be considered from a 3-D perspective [41]. For example, signal switching on the topmost metal layer of a digital plane can produce a noise spike

in an adjacent analog plane bonded in a front-to-front fashion with the digital plane. Considering the different forms of 3-D integration and the various manufacturing approaches, the development of interconnect design techniques and methodologies is a primary focus in high-performance 3-D systems.

Thermal Issues

A fundamental concern in the design of 3-D circuits is thermal effects. Although the power consumption of these circuits is expected to decrease due to the considerably shorter interconnects, the power density will greatly increase since there is a larger number of devices per unit area as compared to a planar 2-D circuit. As the power density increases, the temperature of those planes not adjacent to the heat sink of the package will rise, resulting in degraded performance, or accelerated wear-out mechanisms. Exploiting the performance benefits of vertical integration while mitigating thermal effects is a difficult task. In addition to design practices, packaging solutions and more effective heat sinks are additional approaches to alleviate thermal effects.

CAD Algorithms and Tools

Other classic problems in the IC design process, such as partitioning, floorplanning, placement, and routing, will need to be revisited in an effort to develop efficient solutions that can support the complexity of three-dimensional systems. To facilitate the front-end design process, a capability for exploratory design is also required. For example, design entry tools that provide a variety of visualization options can assist the designer in more easily comprehending and managing the added complexity of these circuits. In addition, as diverse technologies are combined within a single 3-D system, algorithms that include behavioral models for a larger variety of components are needed. Furthermore, the computational power of the simulation tools will need to be significantly extended to ensure that the entire system can be efficiently evaluated.

In this book, emerging 3-D technologies and design methodologies are analyzed, and solutions for certain critical problems are discussed. The next section presents an outline of the book.

1.4 BOOK ORGANIZATION

A brief description of the challenges that 3-D integration faces is provided in the previous section. Several important problems are considered and innovative solutions are presented throughout this

book. In the next chapter, various forms of vertically integrated systems are discussed. Different implementations of three-dimensional circuits at the package and die integration levels are reviewed. Some of these approaches, such as a wire bonded stacked die, have become commercially available, while others have not yet left the R&D phase. Although vertical integration of packaged or bare die offers substantial improvements over planar multichip packaging solutions, the increasing number of inputs and outputs (I/Os) hampers potential performance advancements. This situation is primarily due to manufacturing limitations hindering aggressive scaling of the off-chip interconnects in order to satisfy future I/O requirements.

Consequently, in the third chapter, emphasis is placed on those technologies that enable 3-D integration, where the interconnections between the non-coplanar circuits are achieved through the silicon by short vertical vias. These interconnect schemes provide the greatest reduction in wire length and, therefore, the largest improvement in performance and power consumption. Specific fabrication processes that have been successfully developed for three-dimensional circuits are reviewed.

A theoretical analysis of interconnections in 3-D ICs is offered in the fourth chapter. This investigation is based on *a priori* interconnect prediction models. These typically stochastic models are used to estimate the length of the on-chip interconnects. The remaining sections of this chapter apply the interconnect distributions to demonstrate the opportunities and performance benefits of vertical integration.

The following four chapters focus on issues related to the physical design of 3-D ICs. The complexity of the 3-D physical design process is discussed in Chapter 5. Several approaches for classical physical design issues, such as floorplanning, placement, and routing, from a 3-D perspective, are reviewed. Other important issues, such as the allocation of decoupling capacitance, are also presented.

In the sixth chapter, physical design techniques for 3-D ICs are extended to thermal design and management. Modeling and design methodologies of thermal effects are discussed. Design techniques that utilize additional interconnect resources to increase the thermal conductivity within a multiplane system are emphasized.

Beyond the reduction in wirelength that stems from three-dimensional integration, the delay of those interconnects connecting circuits located on different physical planes of a 3-D system (*i.e.*, the

interplane interconnects) can be further improved by optimally placing the through silicon vertical vias. Considering the highly heterogeneous nature of 3-D ICs that results from the nonuniform impedance characteristics of the interconnect structures, a methodology is described in Chapter 7 to minimize the delay of the interplane interconnects. An interconnect line that includes only one through silicon via is initially investigated. The location of the through silicon via that minimizes the delay of a line is analytically determined. The degradation in delay due to the nonoptimum placement of the 3-D vias is also discussed. In order to incorporate the presence of physical obstacles, such as logic cells and pre-routed interconnects (for example, segments of the power and clock distribution networks), the discussion in this chapter proceeds with interconnects that include more than one through silicon via. An accurate heuristic is described to implement an efficient algorithm for placing the through silicon vias to minimize the overall delay of a multiplane interconnect.

By extending the heuristic for two-terminal interconnects, a near-optimal heuristic for multiterminal nets in 3-D ICs is described in Chapter 8. Necessary conditions for locating the through silicon vias are described. An algorithm that exhibits low computational time is also presented. The improvement in delay that can be achieved by placing the through silicon vias for different via placement scenarios is investigated. For the special case where the delay of only one branch of a multiterminal net is minimized, a simpler optimization procedure is described. Based on this approach, a second algorithm is presented. Finally, the sensitivity of this methodology to the interconnect impedance characteristics is demonstrated, depicting a significant dependence of the delay on the interconnect parameters.

Exploiting the advantages of 3-D integration requires the development of novel circuit architectures. The 3-D implementation of a microprocessor-memory system is a characteristic example of the architectures discussed in Chapter 9. Major improvements in throughput, power consumption, and cache miss rate are demonstrated. Communication centric architectures, such as networks-on-chip (NoC), are also discussed. On-chip networks are an important design paradigm to appease the interconnect bottleneck, where information is communicated among circuits within packets in an Internet-like fashion. The synergy between these two design paradigms, NoC and 3-D ICs, can be exploited to significantly improve performance while decreasing the power consumed in future communication limited systems.

As noted earlier, the distribution of the clock signal in a 3-D IC is an important and difficult task. In Chapter 10, a variety of clock networks, such as H-trees, rings, tree-like networks, and trunk based networks, are explored in terms of clock skew and power consumption to determine an effective clock distribution network for 3-D ICs. A prototype test circuit composed of these networks has been designed and manufactured with the 3-D fabrication process developed at MIT Lincoln Laboratories. A description of the design process and related experimental results are also included in the chapter.

Research on the design of 3-D ICs has only recently begun to emerge. Many of the challenges remain unsolved, and significant effort is required to provide effective solutions to the issues encountered in the design of 3-D ICs. The major foci of this book are summarized in the last chapter and primary conclusions are drawn regarding further directions for research that will contribute to the maturation of this exciting solution to next-generation multifunctional systems-on-chip.

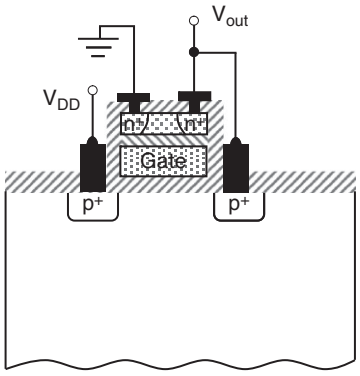
Chapter 2

Manufacturing of 3-D Packaged Systems

With the ongoing demand for greater functionality resulting in polylithic (multiple IC) products, longer off-chip interconnects plague the performance of microelectronic systems. The advent of the system-on-chip (SoC) in the mid-1990s primarily addressed the increasing delay of the off-chip interconnects. Integrating all of the components on a monolithic substrate enhances the overall speed of the system, while decreasing the power consumption. To assimilate disparate technologies, however, several difficulties must be surmounted to achieve high yield for the entire system while mitigating the greater noise coupling among the dissimilar blocks within the system. Additional system requirements for the radio frequency (RF) circuitry, passive elements, and discrete components, such as decoupling capacitors, which are not easily integrated due to performance degradation or size limitations, have escalated the need for technological innovations. Three-dimensional or vertical integration and system-on-package (SoP) have been proposed to overcome many of the inherent SoC constraints. The concepts of vertical integration and SoP are described in Sections 2.1 and 2.2, respectively, as well as the commonality between these innovative paradigms. Several three-dimensional technologies for 3-D packaging are reviewed in Section 2.3. Cost models related to these technologies are described in Section 2.4. The technological implications of 3-D integration at the package level are summarized in Section 2.5.

2.1 THREE-DIMENSIONAL INTEGRATION

One of the first initiatives demonstrating three-dimensional circuits was reported in 1981 [34]. This work involved the vertical integration of PMOS and NMOS devices with a single gate to create an inverter, considerably reducing the total area and capacitance of the inverter.



■ **FIGURE 2-1** Three-dimensional stacked inverter [34].

A cross section of this inverter is illustrated in Figure 2-1. Several other approaches to three-dimensional integration, however, have been developed, both at the package and circuit levels. Bare or packaged die are vertically integrated, permitting a broad variety of interconnection strategies. Each of these vertical interconnection techniques has different advantages and disadvantages. Other more esoteric technologies for 3-D circuits have also been proposed. To avoid confusion, therefore, a crucial differentiation among the various 3-D integration approaches is maintained in this chapter. Two primary categories of 3-D systems are discerned, namely, system-in-package (SiP) and three-dimensional integrated circuits (3-D ICs). The criterion to distinguish between SiP and 3-D IC is the interconnection technology that provides communication for circuits located on different planes of a 3-D system. In SiP, through silicon vias (TSVs) with high aspect ratios are typically utilized. Due to the size of these vias, a high vertical interconnect density cannot be achieved. Hence, these interconnects provide coarse-grain connectivity among circuit blocks located on different planes. Alternatively, in 3-D ICs, fine-grain interconnection among devices on different planes is achieved by narrow and short TSVs.

2.1.1 System-in-Package

Henceforth in this book a system-in-package is described as an assemblage of either bare or packaged die along the third dimension, where the interconnections through the *z*-axis are primarily implemented through the following means:

- Wire bonding
- Vertical interconnects along the periphery of the die/package
- Long and wide, low-density vertical interconnects (in an array arranged across the die/package)
- Metallization between the faces of a 3-D stack

Die or package bonding can be implemented by utilizing a diverse collection of materials, such as epoxy and other polymers. Some examples of SiP structures are illustrated in Figure 2-2. Each example of these manufacturing techniques is discussed in Section 2.3.

2.1.2 Three-Dimensional Integrated Circuits

Three-dimensional IC manufacturing can be conceptualized either as a sequential or a parallel process. In the case of a sequential process, the devices and metal layers of the upper planes of the stack are grown on top of the first plane. Hence, the 3-D system can be treated as a

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